REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1-22 will remain in the application.

Drawings

The drawings were objected to for not showing the pre-decoder recited in claim 14. The drawings have been amended to show pre-decoders 707 in Fig. 5. This change finds support in the Specification at page 12, lines 19-20 and Fig. 5 (showing data lines for pre-decoded 2-bit widths from each of the instruction sources).

Claim Objections

Claim 16 was objected to. Claim 16 has been amended.

Claim Rejections - 35 USC § 102

Claims 1-22 were rejected under 35 U.S.C. 102(a) as allegedly being anticipated by Tran (USP 5,987,235, hereinafter, "Tran").

Applicants teach a processor including an instruction register capable of storing instructions received from multiple instruction sources simultaneously.

Consider exemplary independent claim 1 recites, in relevant part:

"... loading the plurality of instructions into a register, said plurality of instructions including at least one instruction from each of a plurality of instruction sources;..."

Tran does not disclose loading an instruction cache with instructions received from multiple instruction sources. All

instructions come from the instruction cache 204. Accordingly, Applicants submit that claims 1-22 are allowable.

Enclosed is a check for $110.00 for the one month extension fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 04/30/04

Kenyon S. Jenkes
Reg. No. 41,873
Attorney for Intel Corporation

Fish & Richardson P.C.
Customer Number: 20985
12390 El Camino Real
San Diego, California 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10391146.doc